REMARKS

The Examiner is thanked for the thorough examination of the present application and the indication that claims 10-15 contain allowable subject matter. Claims 1-2, 5-6, 10-11, and 14-15 have been amended, and claims 16-18 are newly added. Reconsideration of all rejections is respectfully requested in view of the foregoing amendments and following remarks.

Rejections Under 35 U.S.C. 103(a) of Claims 1-9

Claims 1-9 were rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Lai et al (US 20030049938, hereinafter "Lai") in view of Broermann et al (USPN 20040201858, hereinafter "Broermann") and Kota et al (USPN 20050148104, hereinafter "Kota"). Claim 1 is an independent claim, from which claims 2-9 depend.

Applicant has amended claim 1 to more clearly identify a novel and non-obvious aspect of the invention. Specifically, as amended, independent claim 1 recites:

> 1. A method for process control in an integrated circuit process comprising:
> providing a wafer substrate;
> forming a pad layer on said wafer substrate;
> forming a metal layer on said pad layer;
> patterning said metal layer to form at least one metal plate in at least one region of said wafer substrate;
> milling a plurality of substantially parallel trenches in said at least one metal plate, thereby forming a critical dimension test array wafer; and
> measuring the widths of said parallel trenches therebetween, thereby calibrating said critical dimension test array wafer;
> ***mounting and inserting said calibrated critical dimension test array wafer in a sample chamber of a process control scanning electron microscope;***
> ***calibrating said process control scanning electron microscope by measuring the widths of said trenches therebetween; and***
> ***using said process control scanning electron microscope to measure widths of lines on an in-process integrated circuit wafer.***

(*Emphasis added.*) Amended claim 1 specifically recites **inserting a calibrated critical dimension test wafer for process control thereby forming and calibrating a critical dimension test array and further utilizing it to measure widths of lines on an in-process integrated circuit wafer**. Clearly, amended claim 1 defines over the cited art, as the cited art, wither singularly or in combination, does not disclose or suggest the combination of features emphasized above in amended claim 1. As claims 2-9 depend from amended claim 1, it is Applicant's assertion that these claims are also allowable at least by virtue of their dependency.

Applicant has also amended allowable claim 10 to include a patentably defining feature, and submits that this claim is now in condition for allowance. As claims 11-18 depend from claim 10, these claims are also believed to be in condition for allowance.

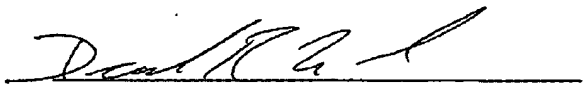
For at least the foregoing reasons, Applicant submits that this application is now in condition for allowance. Prompt issuance of a Notice of Allowance is earnestly solicited.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,



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